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BEAMeeting Southampton

Technical Workshop & Discussion

Welcome to Southampton

- City of Cruise
  - Home of Titanic
    - Wonder of technology & industrial revolution
    - Luxury and status Symbol, Pride of UK
    - “Unsinkable”
  - - Still home cruises to all over the world

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  - Home of Titanic
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    - “Unsinkable”
  - - Still home cruises to all over the world
- Home of Technology
  - Southampton University with >150a history
  - Spitfire airplane impact on 2nd world ware
  - Innovation of glass-fiber in 70th enabled optical communication
  - One of major photonic research hubs and nanofabrication center

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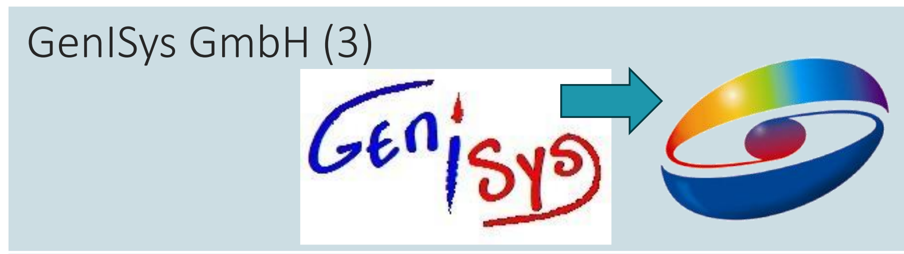
GenISys founding years

2005 / 2006

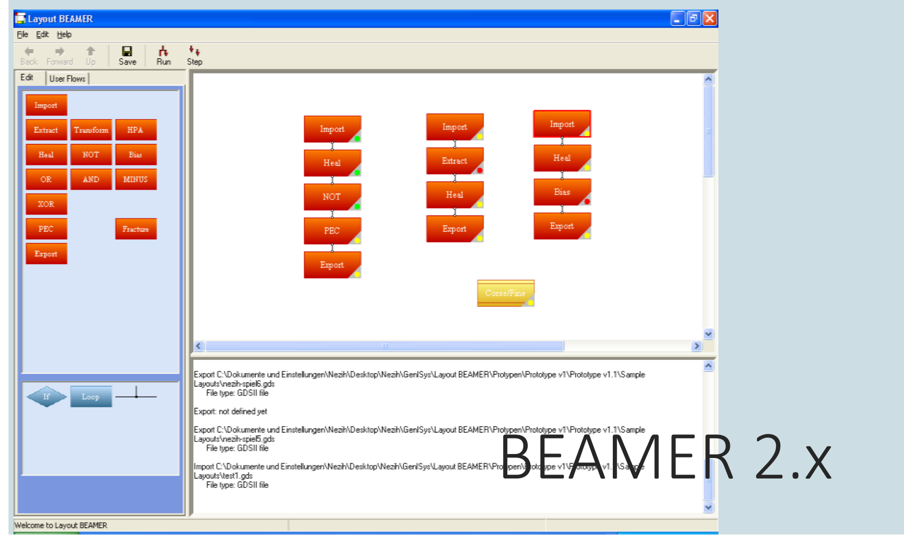
GenISys GmbH (3)



10 licenses total

1st BEAMER license

9 Engine



BEAMER 2.x

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1st BEAMeeting at MNE 2009

„Local“ BEAMeetings

BEAMeeting 2010 Southampton
Technical Workshop & Discussion

Date: March 9th (Tuesday), 20010, Time: 10:00h-16:00h

Location: University Southampton, School of Electronics and Computer Science
Contact person: Martin Charlton (mdbc@ecs.soton.ac.uk)
Directions: http://www.ecs.soton.ac.uk/about/getto.php

Invitation &Program

BEAMeeting2011 Paris
Technical Workshop & Discussion

Date: **Thursday March31st , 2011**
Start: 10:00 am
End: 17:00 pm

Location: CNRS / LPN Laboratoire de Photonique
route de Nozay
91460 MARCOUSSIS
France

BEAMeeting2010 Beijing
Technical Workshop & Discussion on E-beam Lithography
电子束光刻技术研讨会
"Layout BEAMER"和"Layout_LAB"电子束光刻数据处理与模拟技术交流
１０月２６日（星期二）

地点：北京市朝阳区北土城西路３号中国科学院微电子研究所二楼会议室
时间：上午 9:00-11:30；下午 1:00-5:00（215 会议室）
联系人：陈宝钦 chenbq@ime.ac.cn；李新涛 lixintao@ime.ac.cn

Program

	Tuesday October 26,2010	Start
Prof. Chen （IMECAS）	Welcome –Introduction 致欢迎辞	9:00
John Sachen （GenISys）	**GenISys Introduction GenISys 公司简介**	9:30
Nezih Unal （GenISys）	**E-Beam Lithography: From Layout to Wafer** Techniques for layout processing and fracturing **电子束光刻技术：从版图布局到硅片直写**	9:45
Peixiong Shi 史佩雄先生 （DTU / DANCHIP）	**电子束**	
Nezih Unal （GenISys）	Electro 电子散	

BEAMeeting – 14th November 2011
Technical Workshop & Discussion

The BEAMeeting will be hosted by :

California Institute of Technology (CalTech)
Pasadena, CA 91125

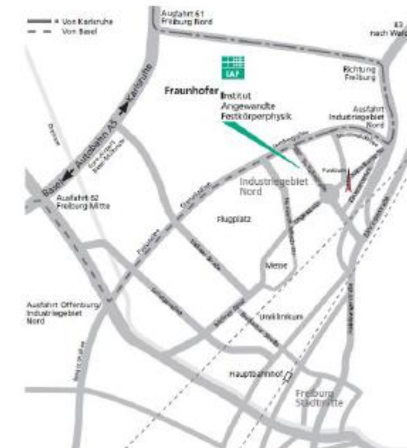
Contact Person: Guy A. DeRose - e-mail: derose@caltech.edu

BEAMeeting 2010 Freiburg
Technical Workshop & Discussion

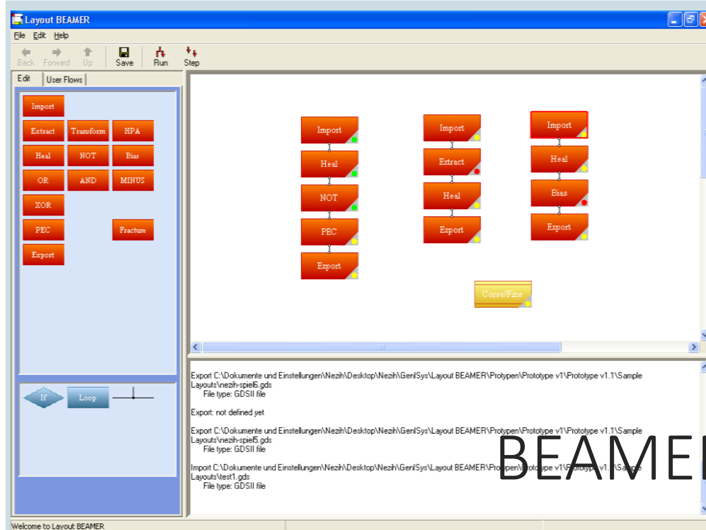
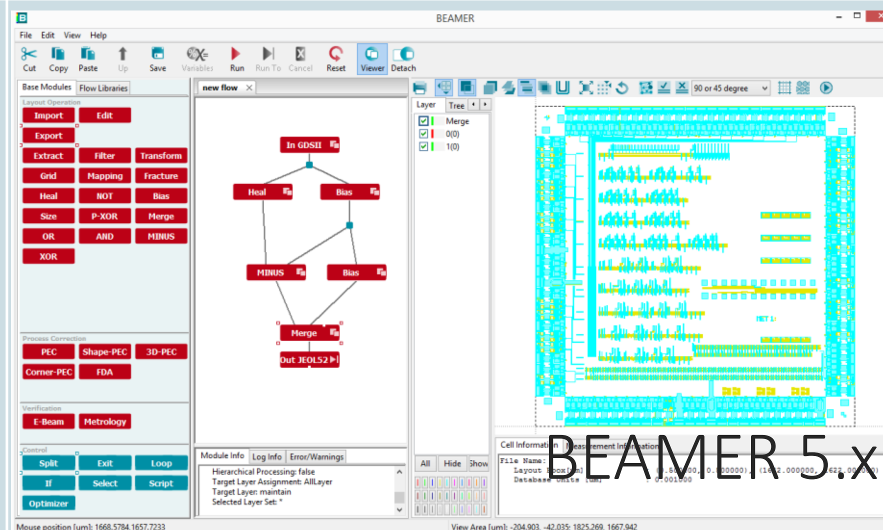
Date: March 17th (Wed), 20010, Time: 10:00h-16:00h

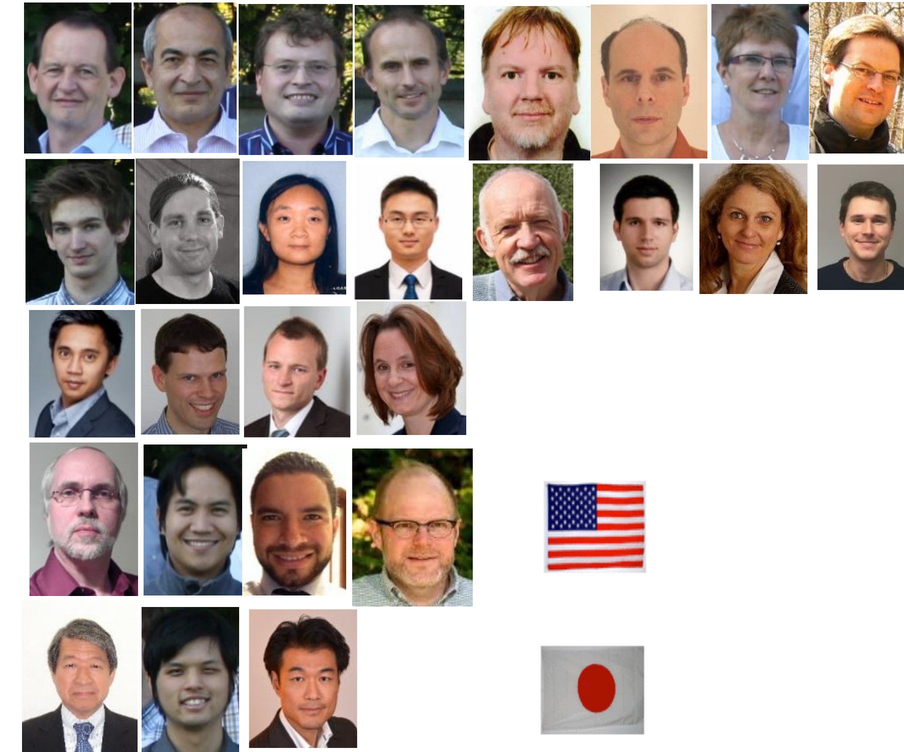
Location: Fraunhofer IAF, Tullastr. 72, D-79108 Freiburg, Germany
www.iaf.fraunhofer.de

From the South:
Autobahn A5 Basel-Karlsruhe, exit 62 „Freiburg-Mitte“, towards Freiburg, 3rd exit „Offenburg / Industriegebiet Freiburg-Nord / Landwasser“, turn right at the 4th exit into Tullastrasse.

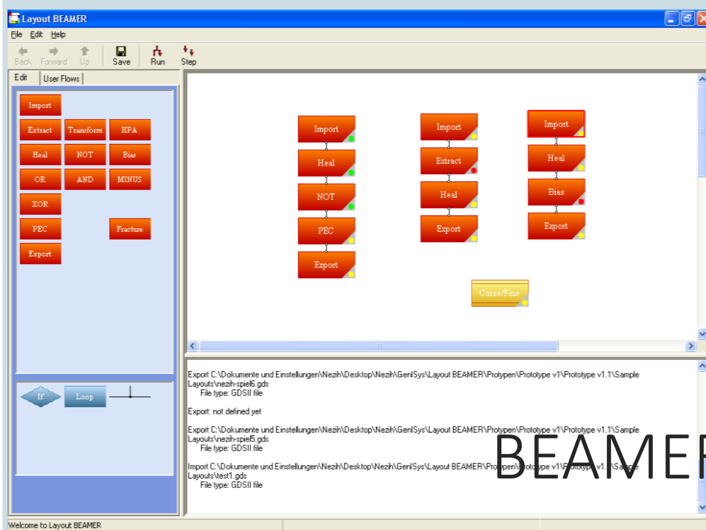
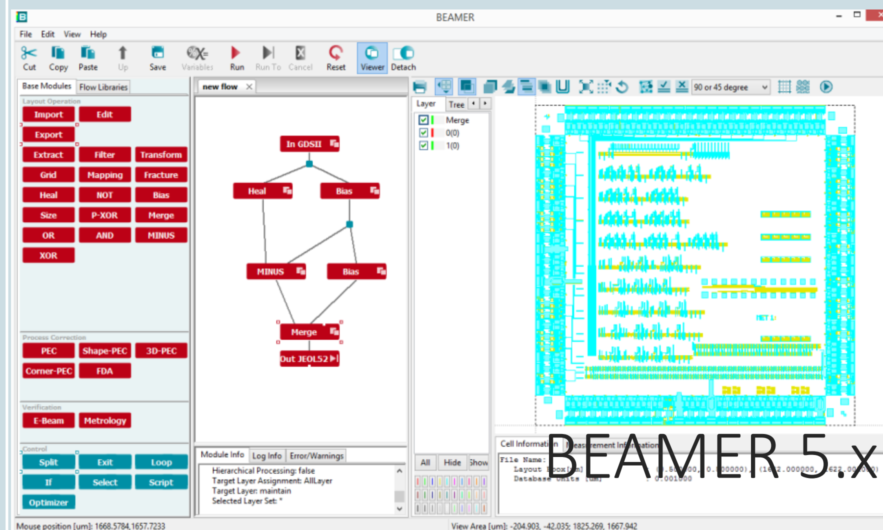
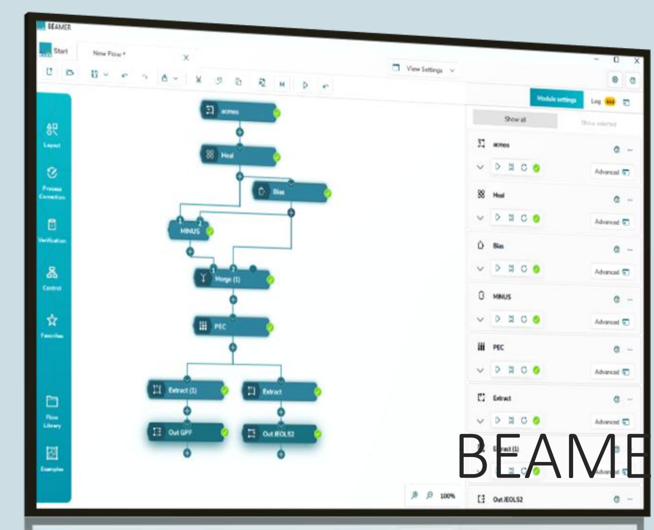


GenISys 2015

2005 / 2006	2015
GenISys GmbH (3)	GenISys GmbH (20) GenISys KK (3) GenISys, Inc. (4)
10 licenses total 1st BEAMER license 9 Engine	282 licenses total 142 BEAMER 69 TRACER 40 LAB 31 Engine
 BEAMER 2.x	 BEAMER 5.x



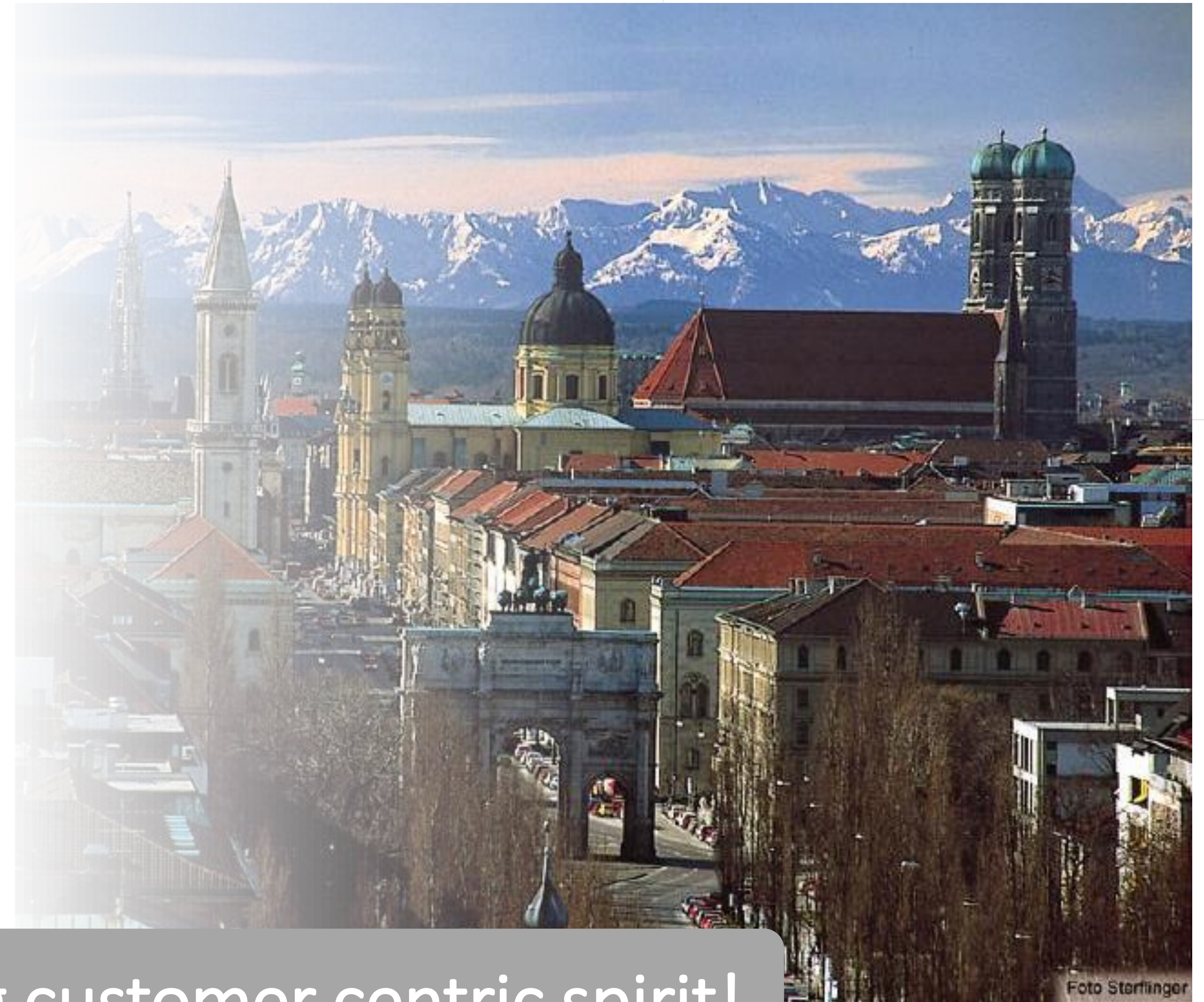
GenISys today

2005 / 2006	2015	2025
GenISys GmbH (3) 	GenISys GmbH (20) GenISys KK (3) GenISys, Inc. (4)	GenISys GmbH (54) GenISys KK (4) GenISys, Inc. (3) GenISys AS (19)
10 licenses total 1st BEAMER license 9 Engine	282 licenses total 142 BEAMER 69 TRACER 40 LAB 31 Engine	1100+ licenses total 460 BEAMER 320 TRACER 110 LAB 135 ProSEM …
		

About GenISys

GenISys offers software solutions for the optimization of micro- and nano-fabrication processes

- Founded in 2005 in Munich, Germany
  - Joined RSBG Group LAB14 in 2018
- Headquarter in Unterhaching, Munich
  - Global organization with >70 employees
  - Subsidiaries in USA, Japan, and Turkey
  - Development locations in Jena, Erlangen, Urla
- Worldwide leader on proximity and process correction for electron and laser lithography



GenISys continues to grow while maintaining customer centric spirit!

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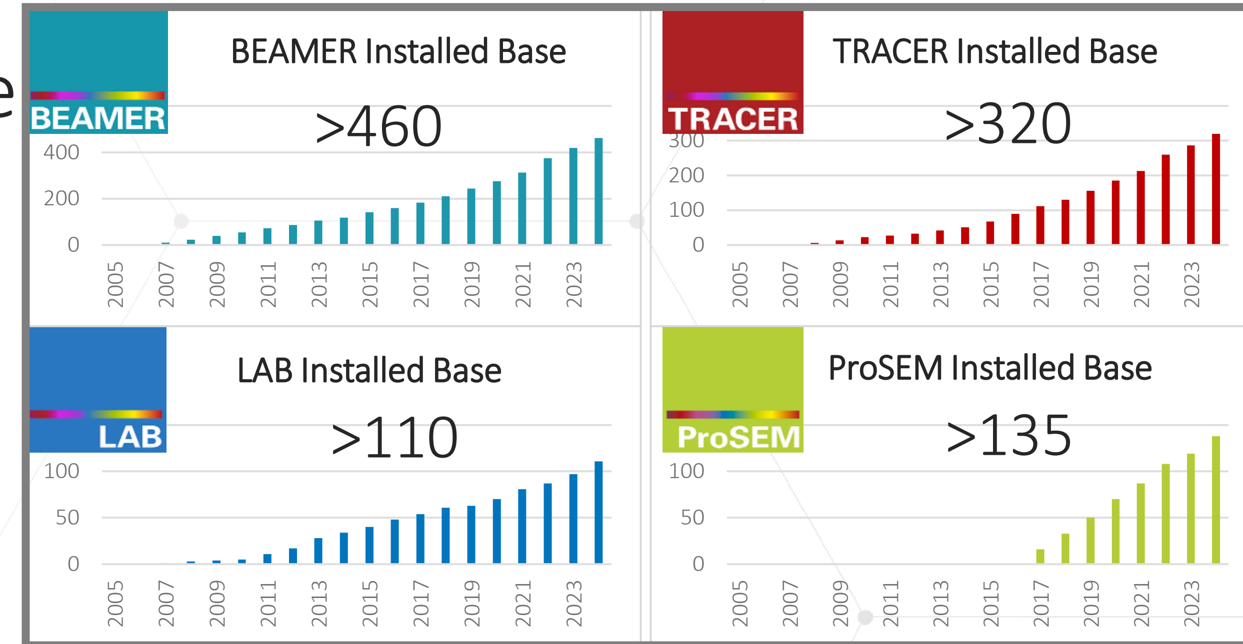
Selected Installed Base: 1100+

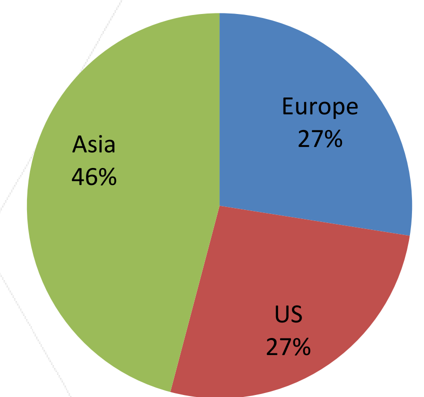
- Major nanofabrication centers worldwide
  - Universities, Research Centers
- Industrial R&D and special production
  - Advanced FPD manufacturers
  - Mask manufacturer
  - Leading IDMs



Europe – Middle East

Asia

North America



Strategic Partnerships

GenISys is an independent software supplier working with all major lithography and inspection system manufacturers.

Welcome to our Equipment Partner

Thanks to our equipment partner for the good cooperation which is essential for good results. Please use the opportunity interacting with them for exchange ….

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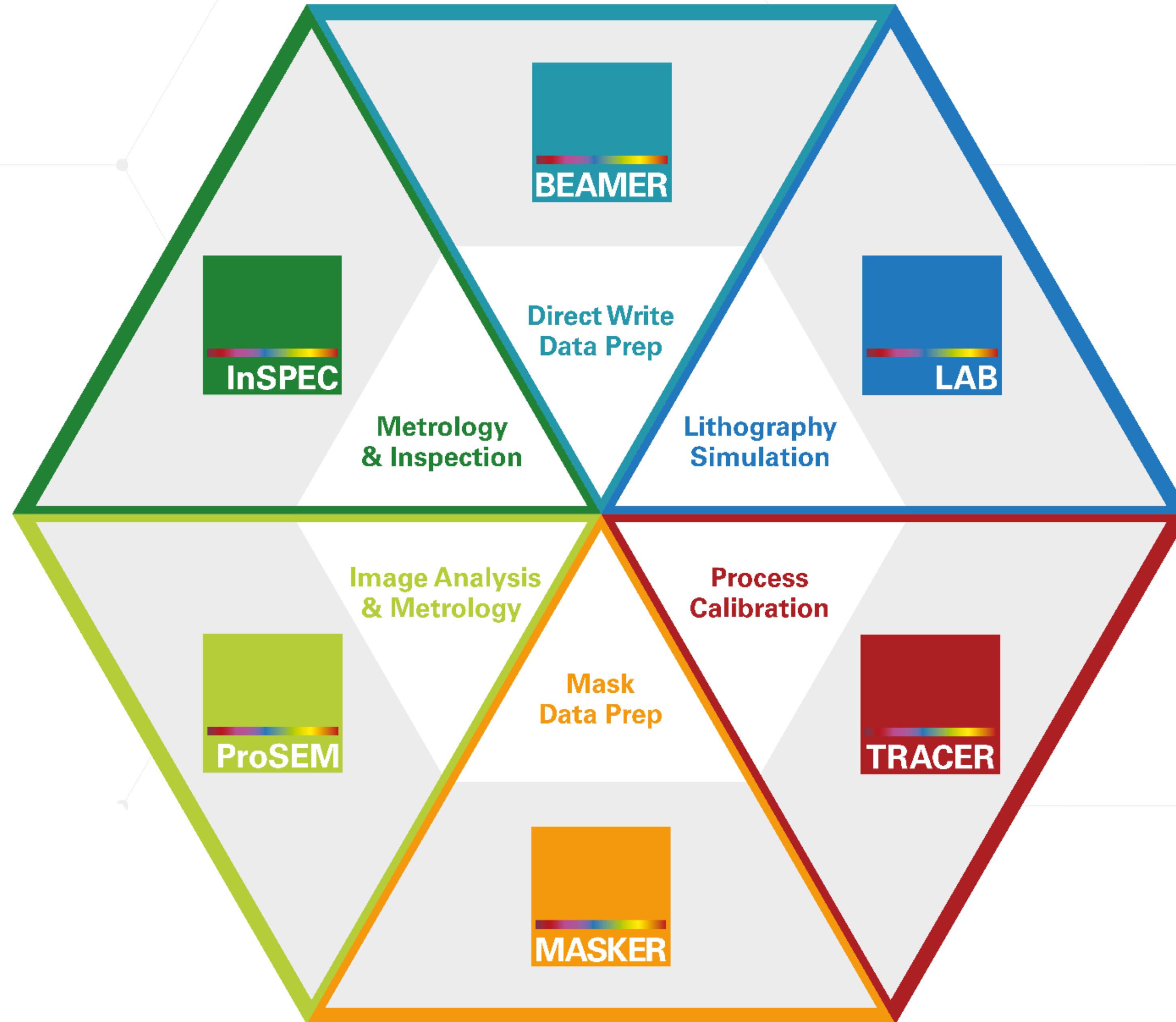
Product Portfolio



Product Portfolio

Direct Write Data Prep
BEAMER
Metrology & Inspection
InSPEC
Lithography Simulation
LAB
Image Analysis & Metrology
ProSEM
Process Calibration
TRACER
Mask Data Prep
MASKER

- Electron and Laser Beam Direct Write Software
- Installed at most major nano-fabrication centers worldwide, has become a MUST for advanced e-beam lithography

- MC-Simulation of electron distribution for e-beam lithography modeling and correction
- Process Calibration, PSF visualization, extraction and management

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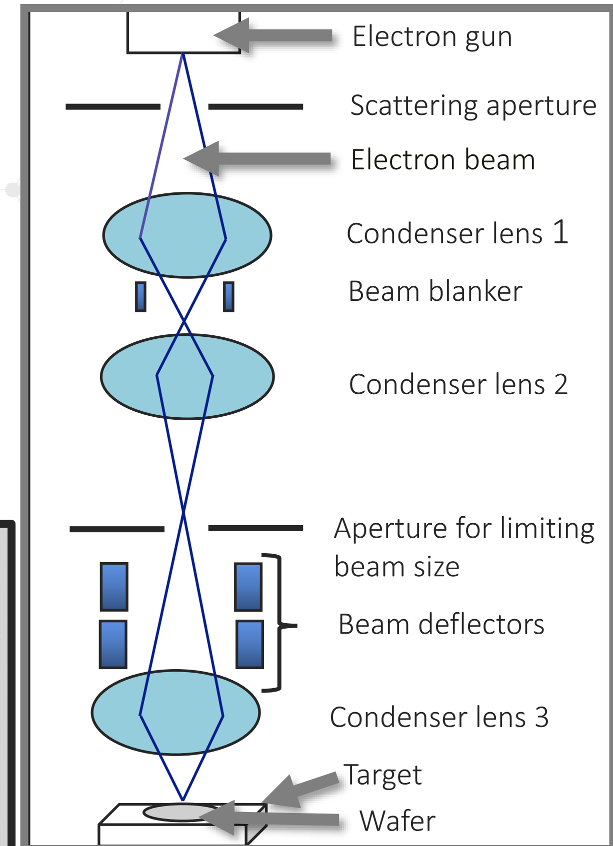
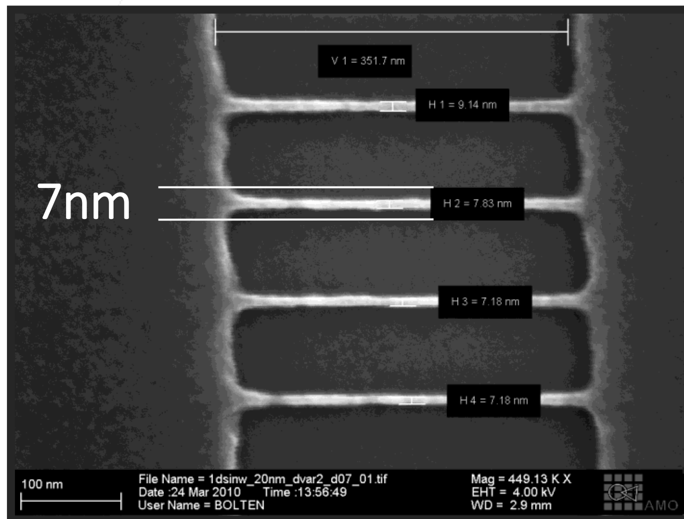
Electron Beam Lithography

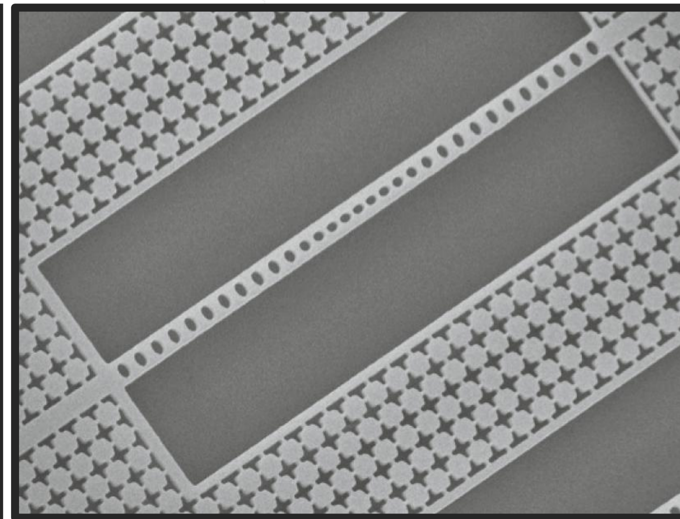
E-Beam lithography (EBL) is the most utilized technology for patterning nano-scale (Quantum) devices

- Beam size down to few nano-meter
- Most flexible pattern and substrate
- Direct Write from CAD data to sample

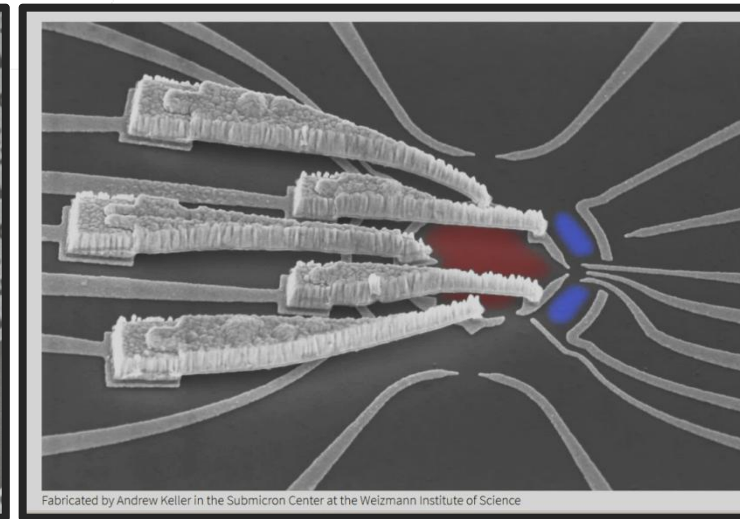




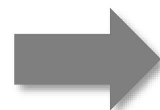
Source: AMO GmbH - Germany



Source: NIST CNST - USA



Source: Weizmann Institute – Israel
Stanford University, USA

GOOD DATA IN  GOOD SAMPLE OUT

Easy, Fast and Accurate Direct Write Litho

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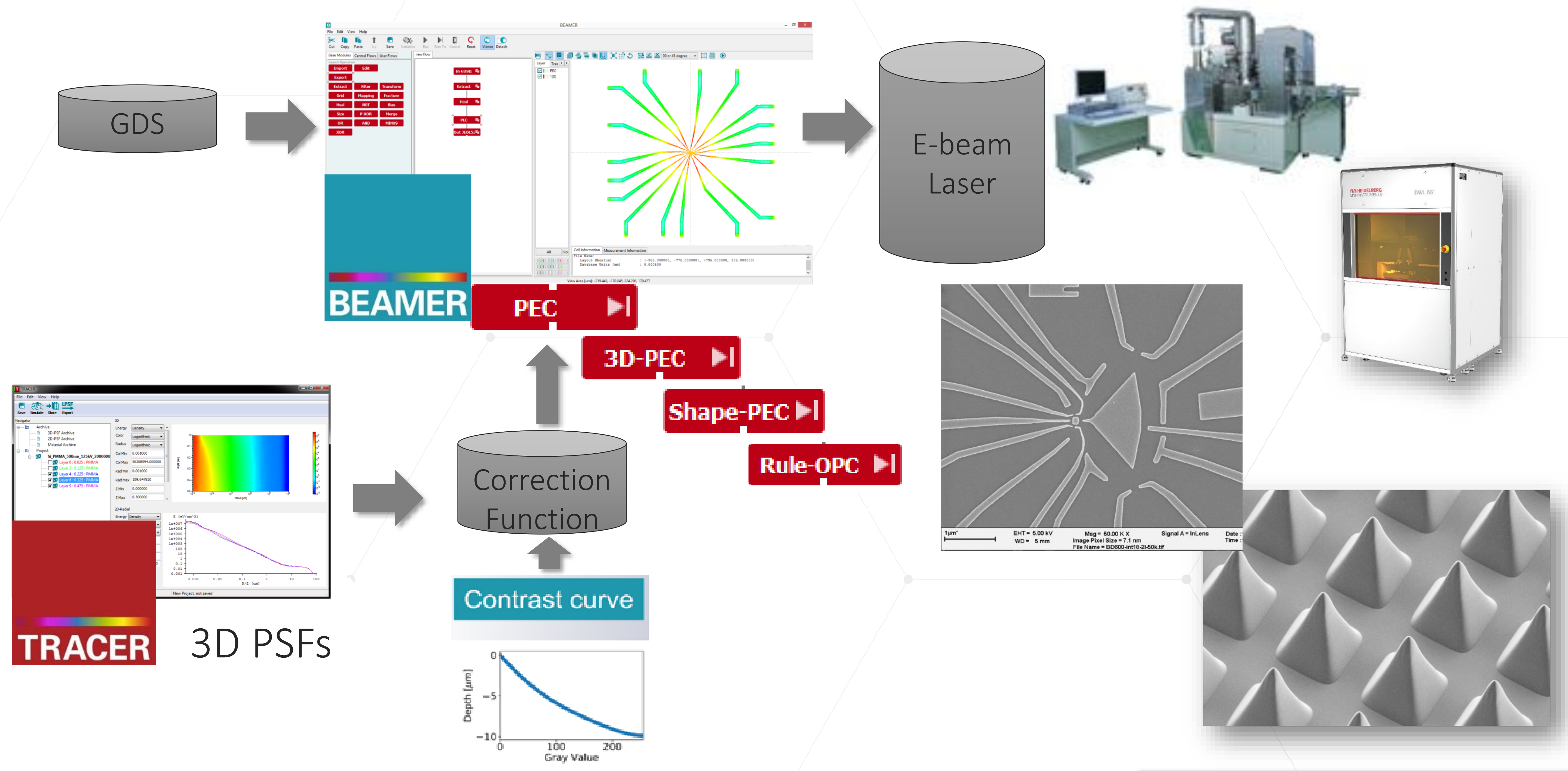
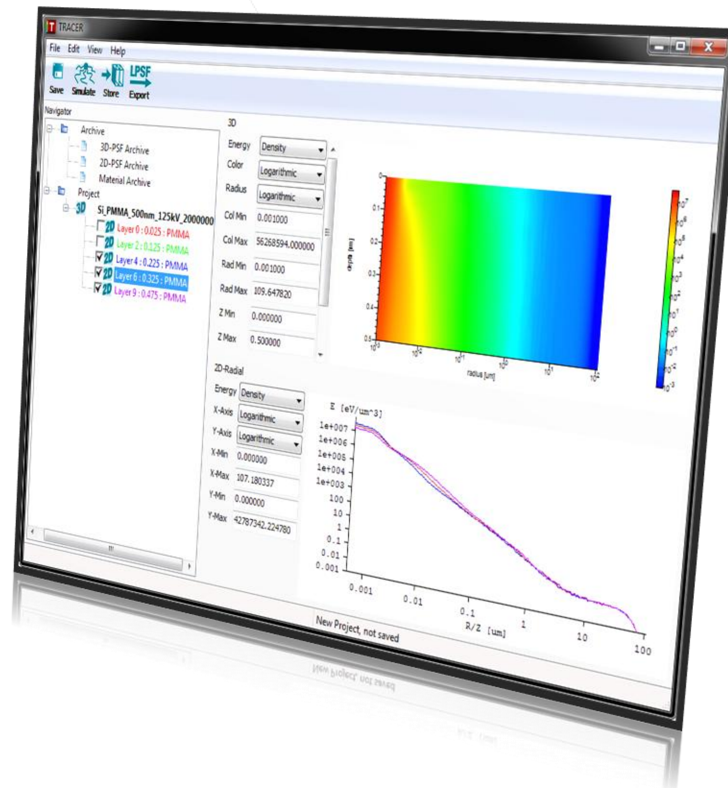


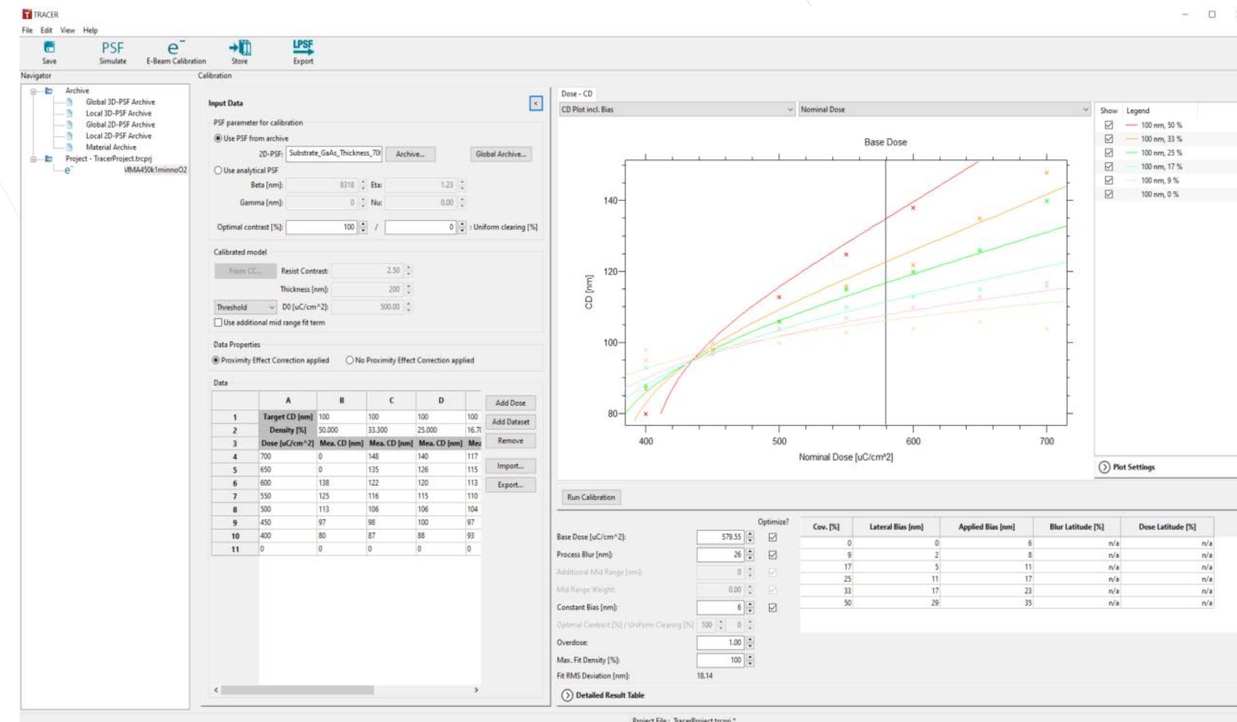
TRACER – PSF & Process Calinration

TRACER calculates PSF by MC simulation

TRACER enables to identify the optimal process point in a simple experiment

- proven for multiple substrates (Si, SiO2, GaAs, InP, …)
- proven for typical direct write resists (PMMA, ZEP, HSQ, CARs …)

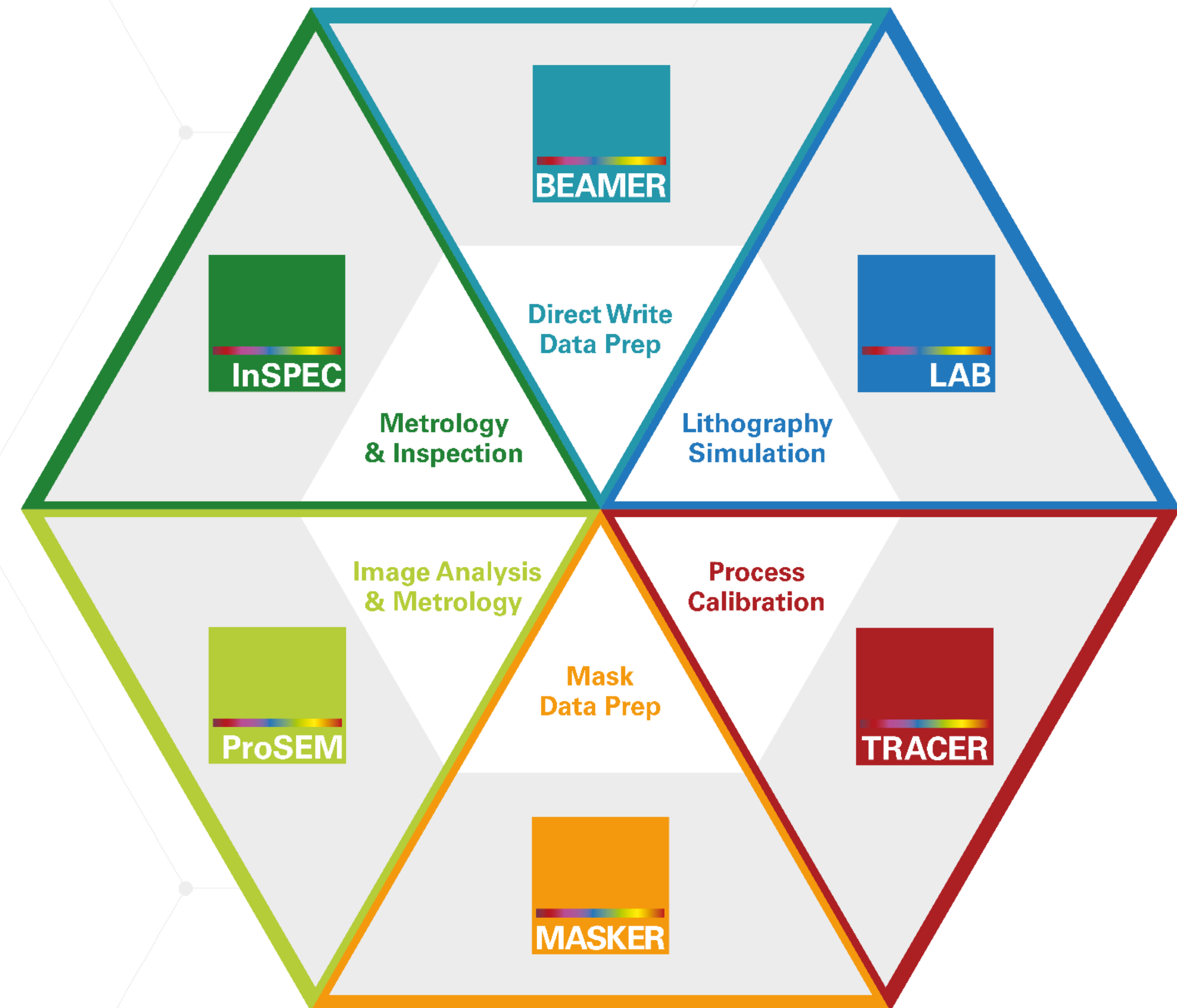




Product Portfolio

- Integrated layout-based SEM metrology and inspection upgrade kit
- Versatile software suite with modular flows for expert measurements

- Image analysis and metrology software for lithography and nanostructures
- Layout-based metrology and image acquisition with SEM tool external control



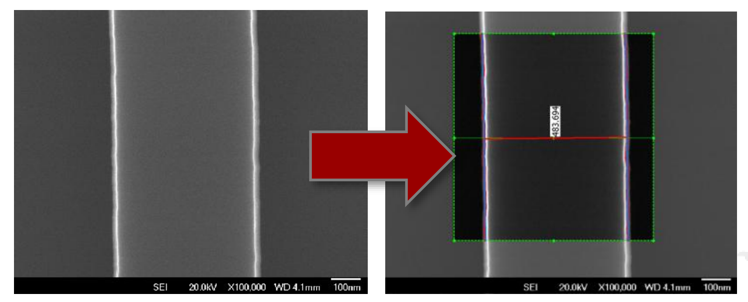
SEM Metrology Scenarios

Offline SEM Image Metrology

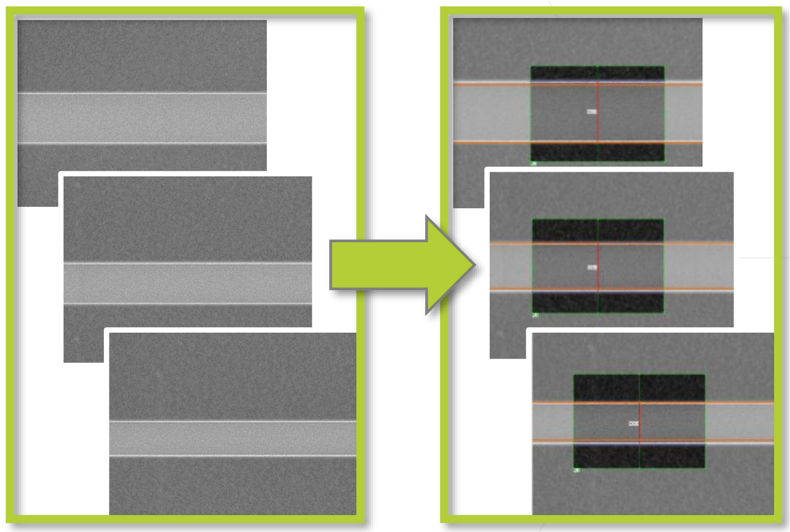
External SEM Control and Image Metrology

Integrated Automation for SEM Metrology

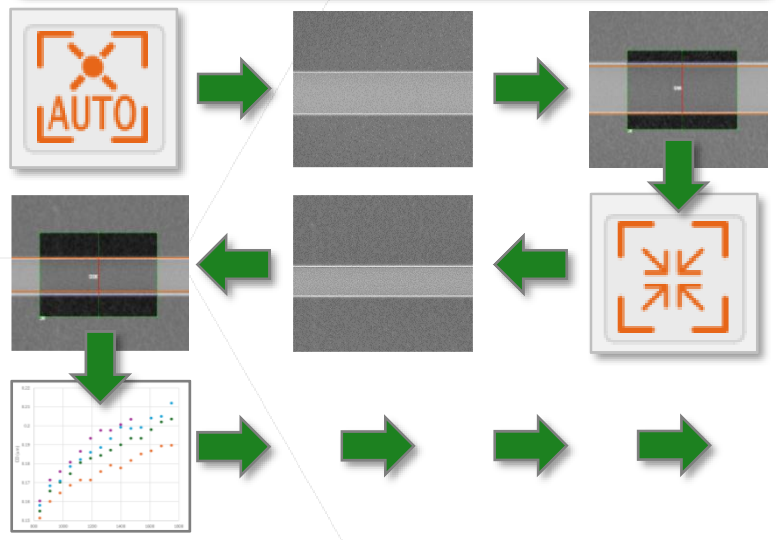
SEM
ProSEM



SEM
ProSEM
ProSEM



InSPEC
SEM



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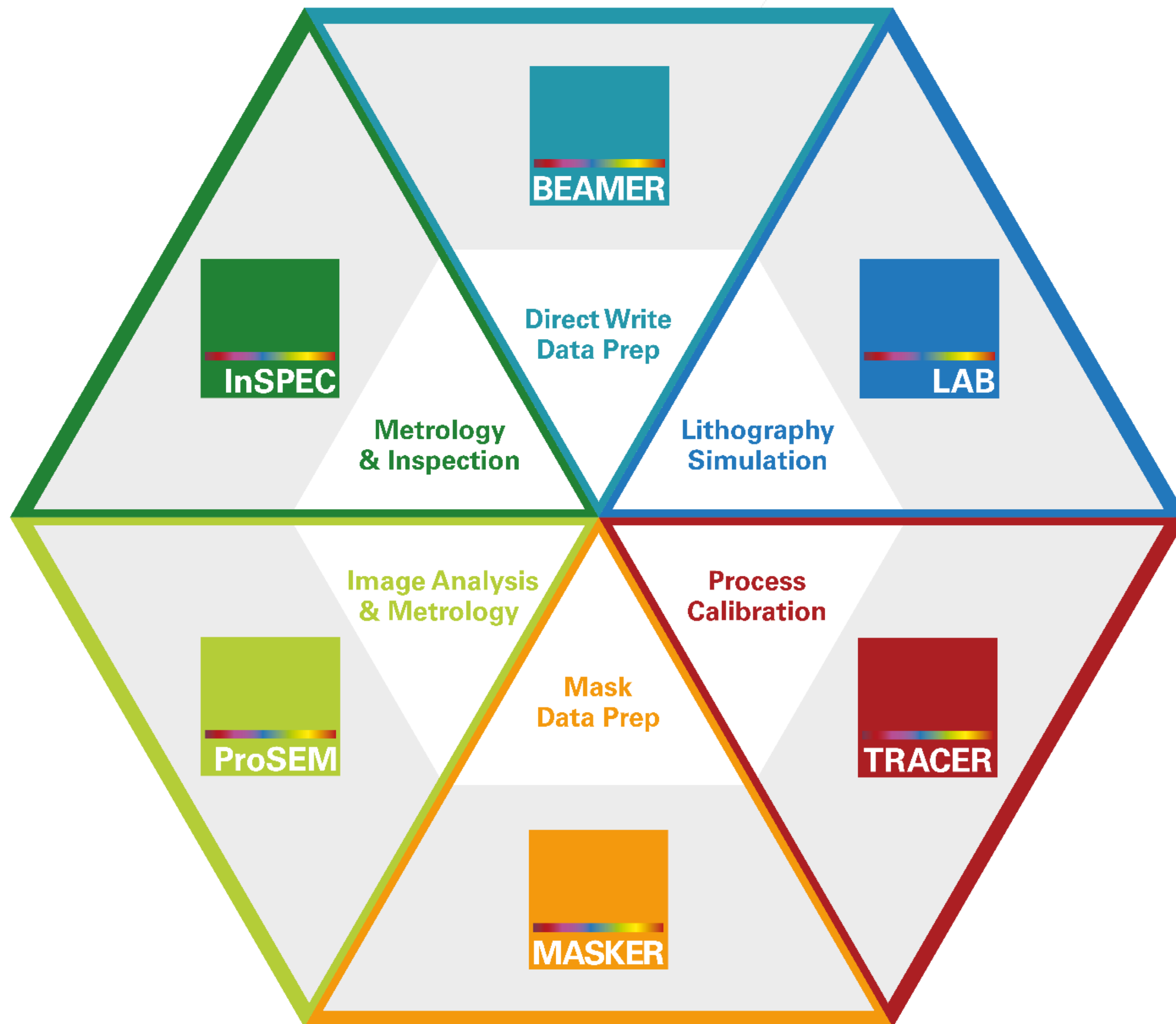
Product Portfolio



- 3D lithography simulation and OPC software
- Proximity Lithography & Projection Lithography
- Electron Beam Lithography & Laser Beam Lithography (Heidelberg Instruments)

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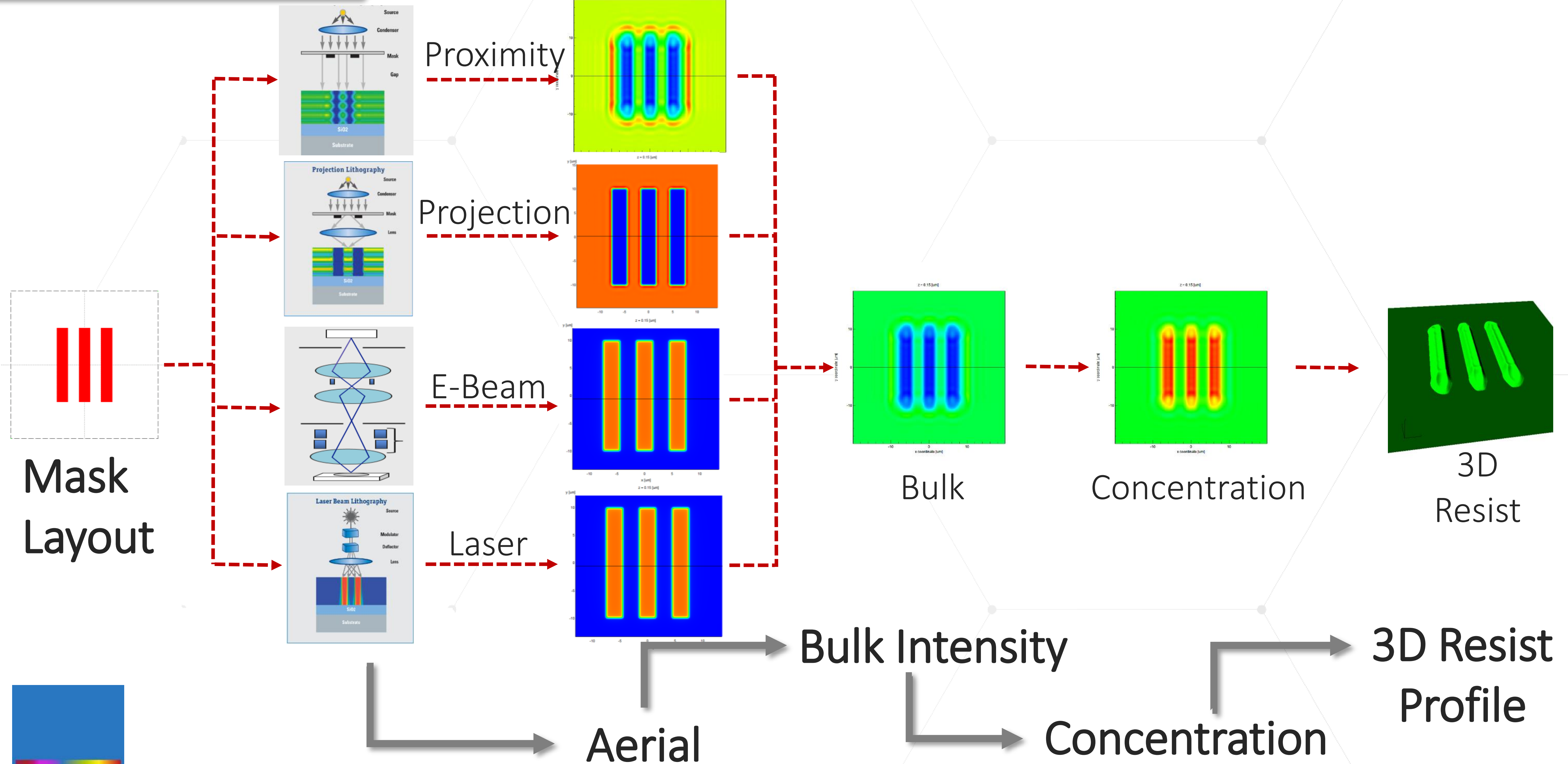
Simulation Flow



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Intensity Image Analysis

Projection Exposure

Mask | Stack | Tool | Simulation | Analysis | Label/Comment

Spectrum

Predefined Spectrum: 365 nm (i-line)

Wavelength [nm]	Rel. Weight	Peak Width [nm]
365	1	5

Import ... | Export ... | Delete Row

Exposure Dose [mJ/cm^2] 2.5

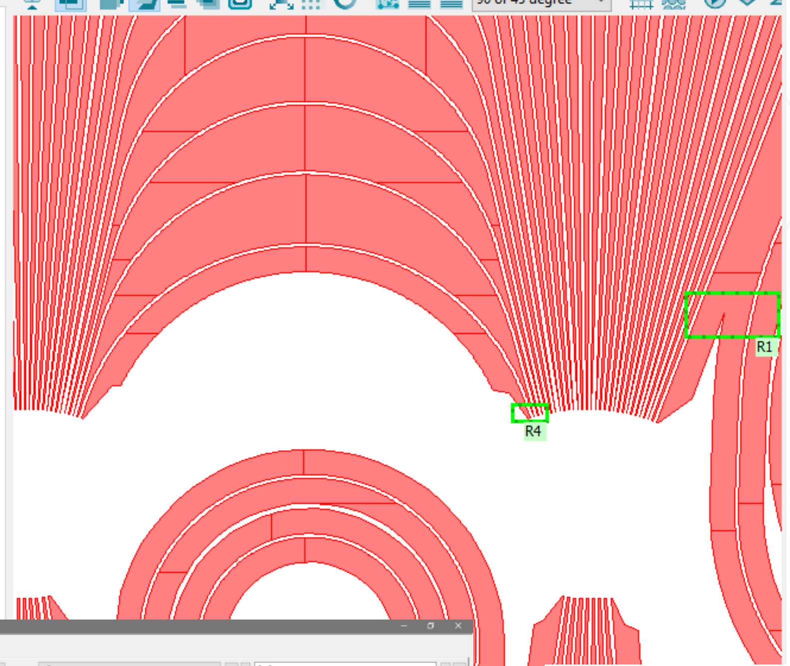
Polarization Scalar

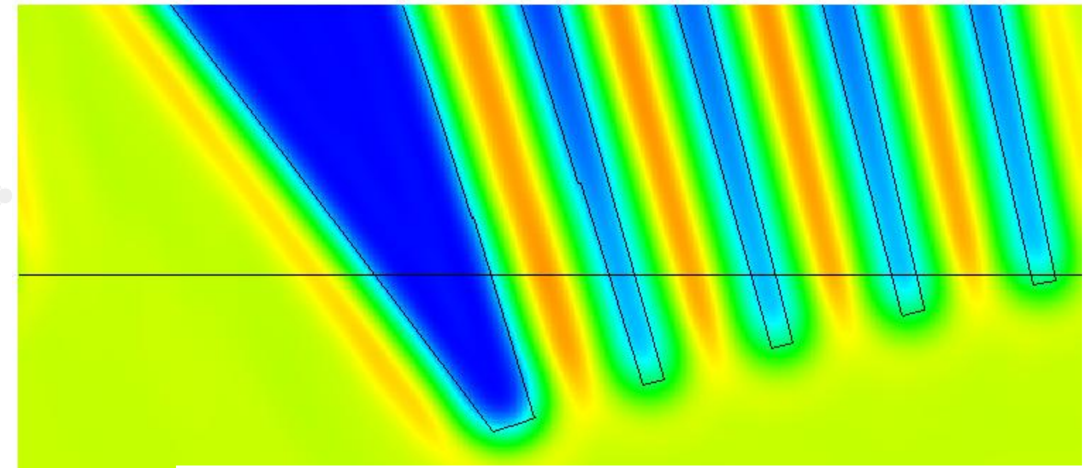
Source

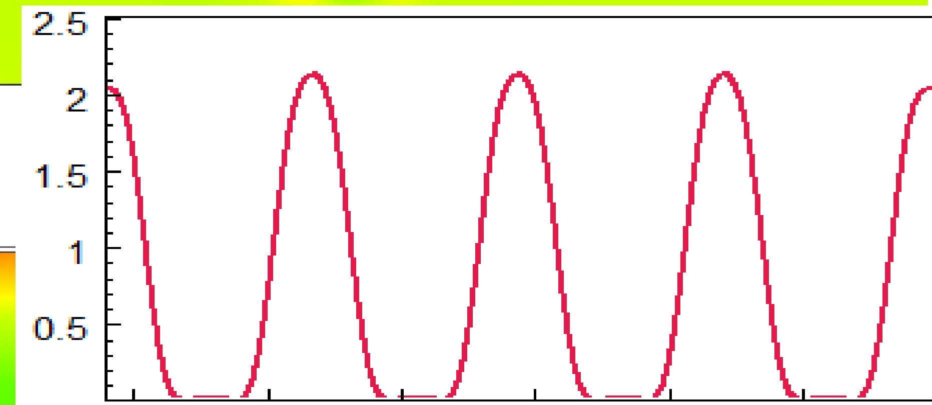
Type Annular
Sigma 0.500000
Sigma 2 0.250000
Annular Fixing 0.000000

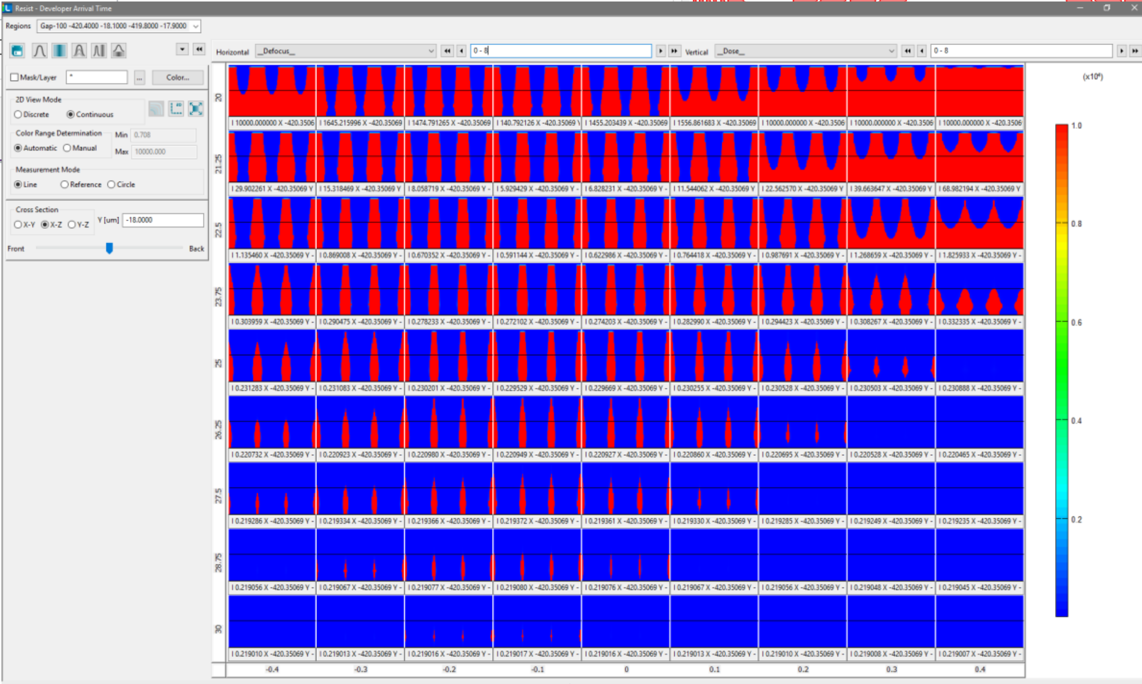
Exposure Parameters

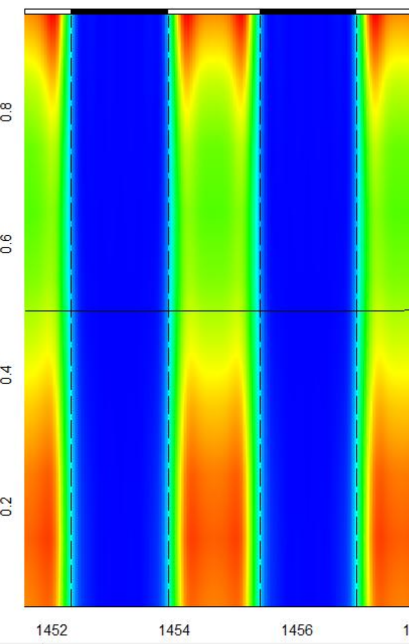
Focus Offset [um] 0.000000 | Focus Pos. Stack top | Immersion Index 1.000000
Defocus direction Away from substrate | NA 0.3 | Reduction 1.000000
Flare Background 0.000000
Aberrations

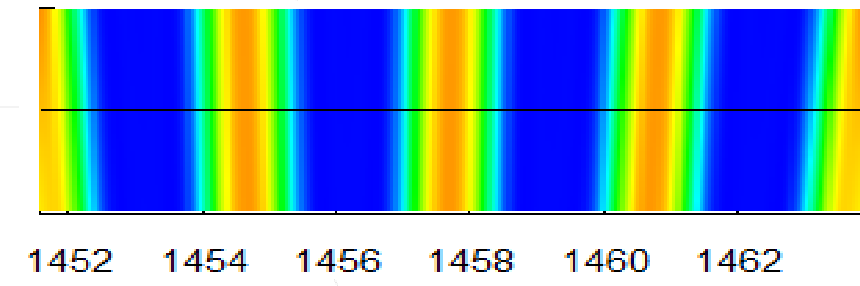








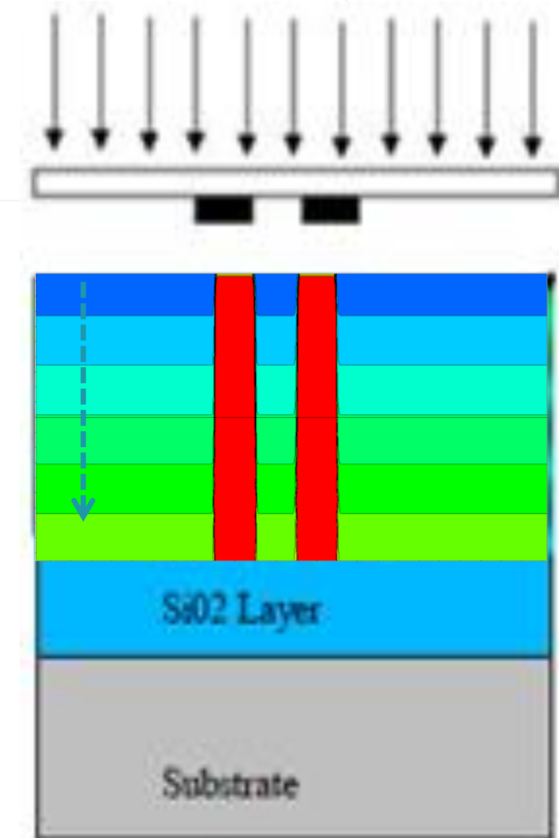




3D Resist Modelling

3D resist development model based on development rate model parameter:

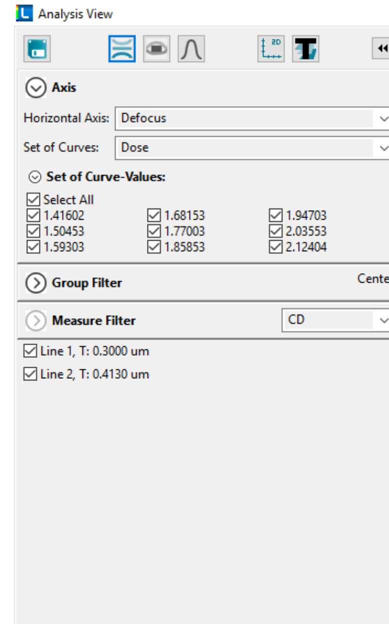
- Bulk image intensities are converted in concentrations
- Concentrations define dissolution rate
- The 3D development front over is modeled over development time
  - Threshold / Diffused Threshold
  - MACK 4 Model
  - CAR Model
  - Development Rate (Contrast Curve)

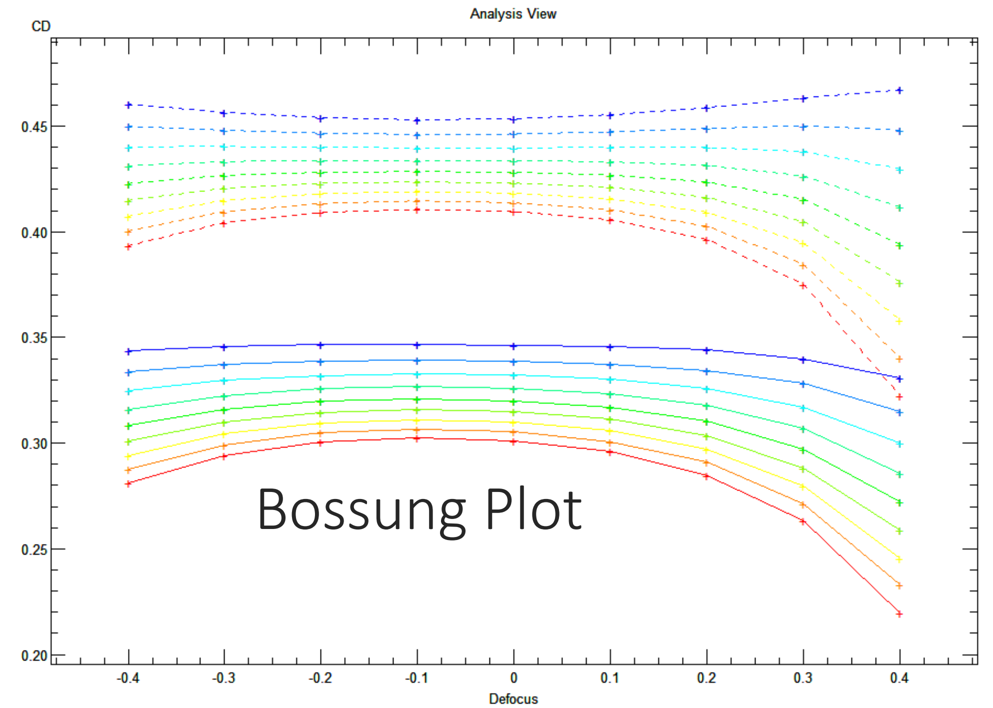


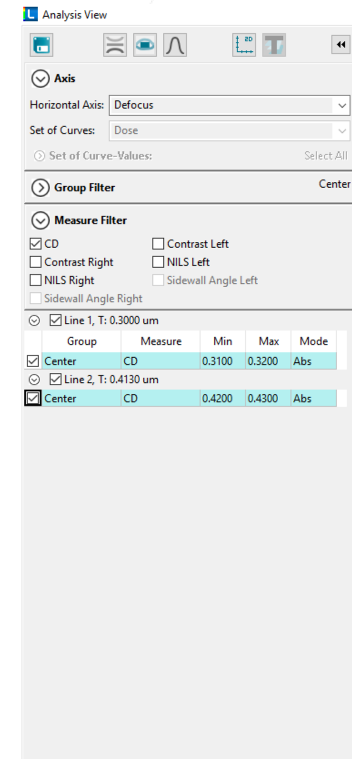
Process Analysis Features

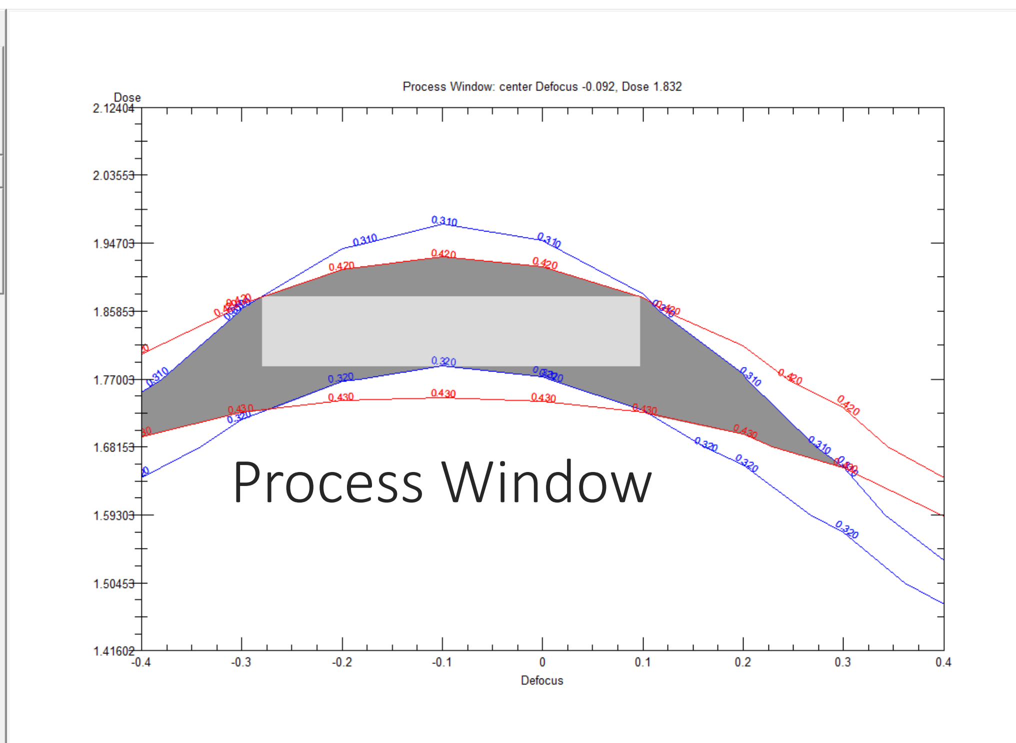
Easy to use analysis capabilities

- Focus-Exposure-Matrix
- Process Window
- Overlapping Process Window



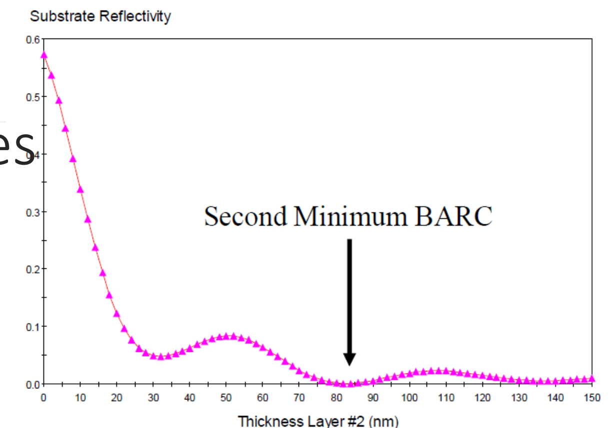






Film stack optimization minimizing standing waves

Type	Material	Thickness [um]
Resist	Ultra_i123	0.3
ARC	AZ_BARLi_II	0.2
Layer	SiO2	0.12
Substrate	Si-crystalline	--



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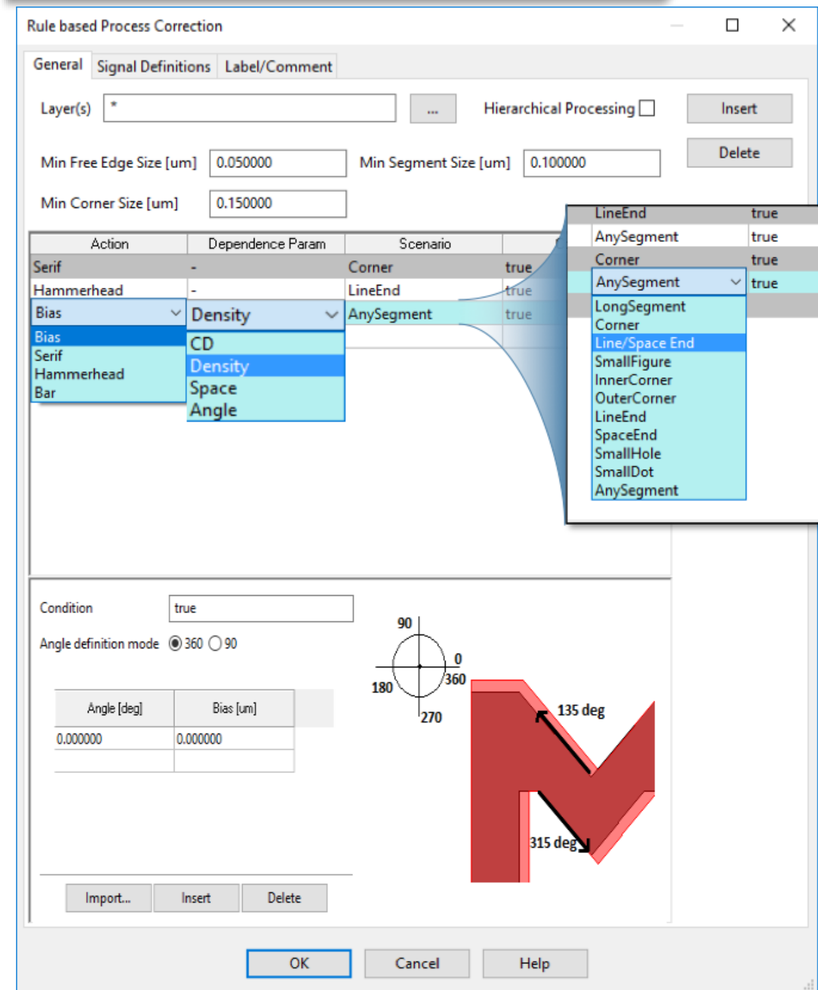
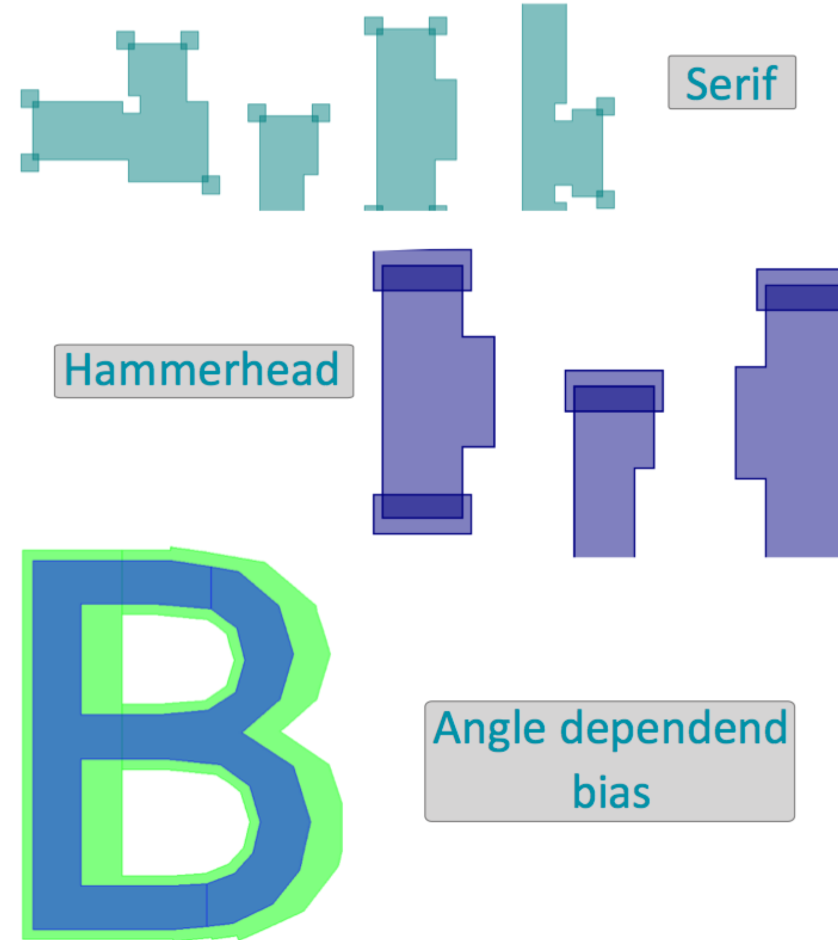
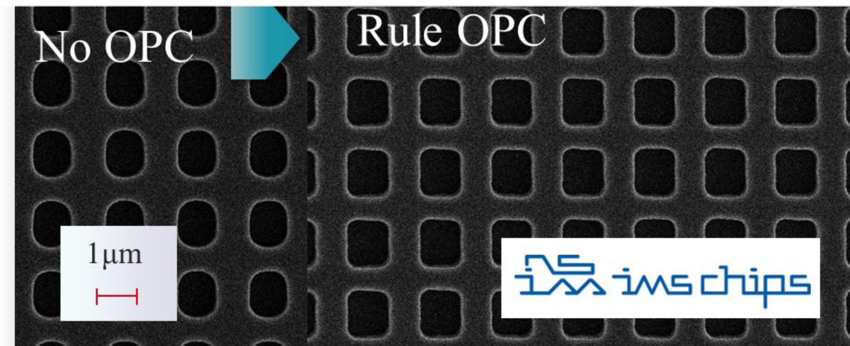
Rule-based OPC







Rule Based: Shape fidelity correction on 0.9 µm squares

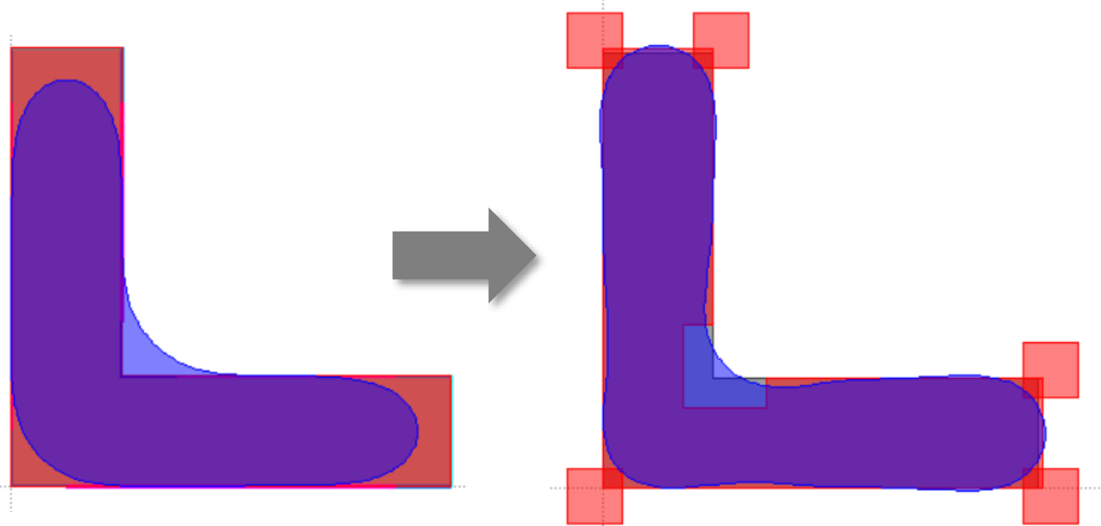
Rule-based proximity correction:

- Variable bias
  - Depending on angle, size, density, space, distance/proximity
- Serifs, hammerheads and bars can be applied based on user-defined rules
- Applicable to all exposure techniques (laser, mask aligner, projection, e-beam)

Rule based correction with simulation

example01
prj-02
Resist
Rule-OPC

Rule-OPC connected after simulation module allows to **preview** simulation contour together with correction and optimize correction parameters



Update Preview

To optimize parameter use this syntax: %[lower_bound:upper_bound]%.

Start Optimizer

Rule based Process Correction

General | Advanced | Signal Definitions | Label/Comment

Min Free Edge Size [um] 0.050000
Min Segment Size [um] 0.100000
Min Corner Size [um] 0.150000
Max Segment Size [um] 1000000.000000
Bias Limit [um] 0.000000
Target Layer OPC

Action	Dependence Param	Scenario	Condition	Optimize
Bias	CD	LineEnd	true	☑
Serif	-	OuterCorner	true	☑
Bias	CD	InnerCorner	true	☑
				☐

Insert
Delete
Up
Down

Condition true

CD [um]	Bias [um]
)00000	%-[0.02:0.1](-0.050409)%

Import... Insert Delete

Bias

To optimize parameter use this syntax: %[lower_bound:upper_bound]%.

Start Optimizer Stop Optimizer

OK Cancel

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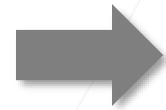
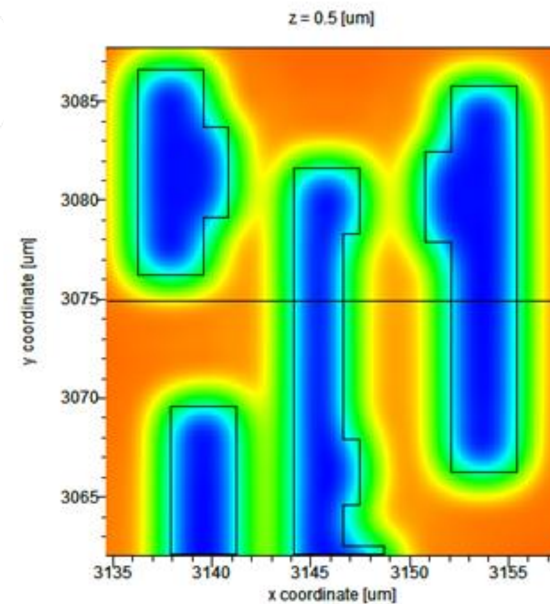
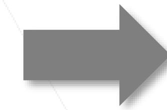
Model Based OPC for Projection

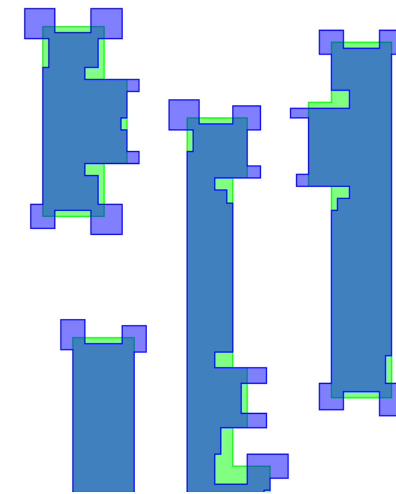
Fully automated OPC correction using :

- The exposure is modelled at layout edges (fast simulation), compared to target, the layout is modified (shape correction) to compensate for mismatch
- Special: Any angle implementation, user defined priorities









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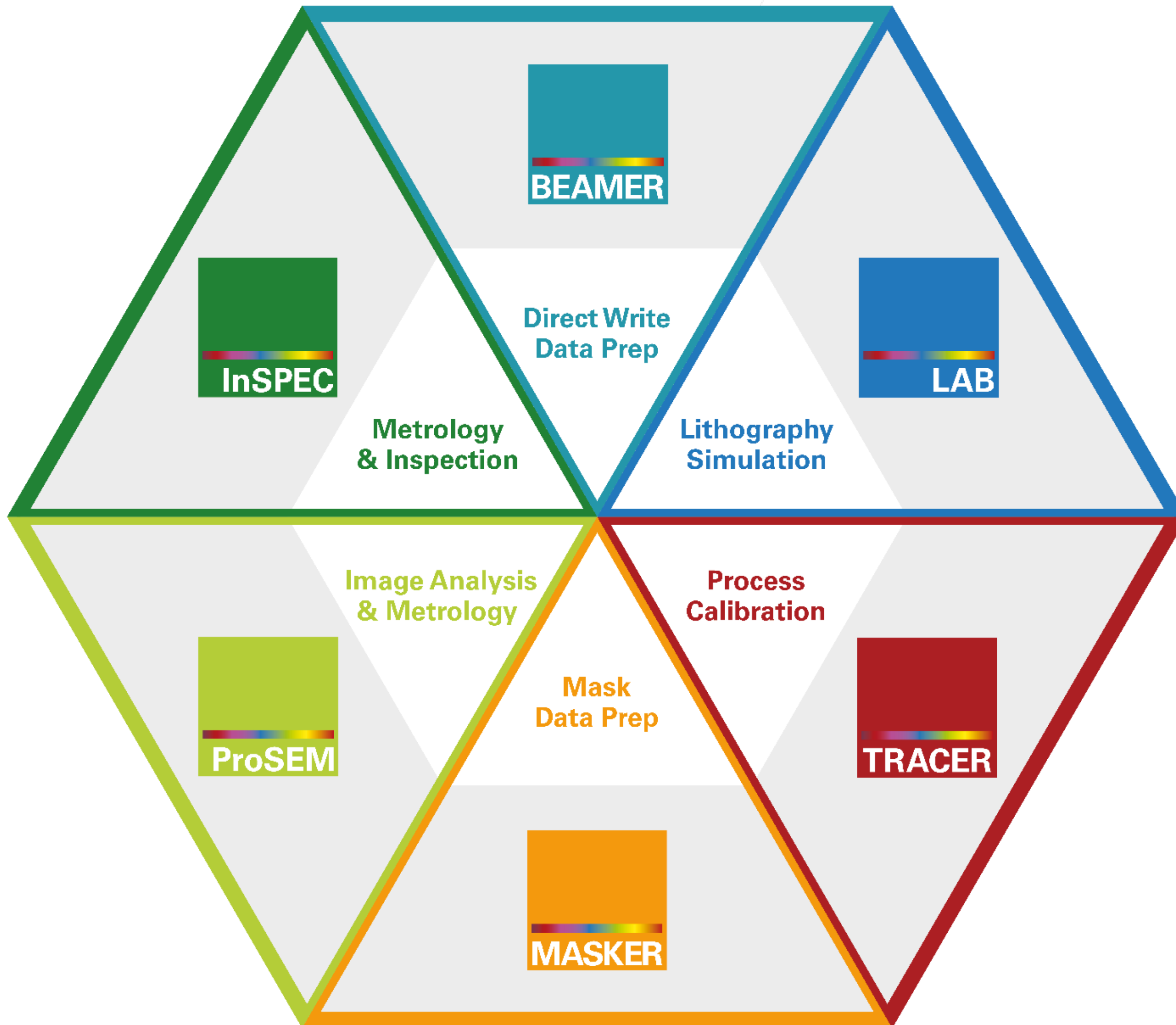
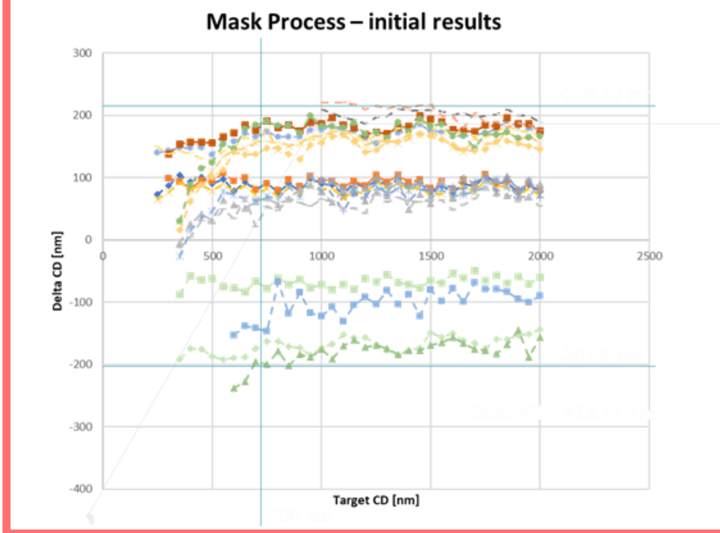
Mask Data Preparation

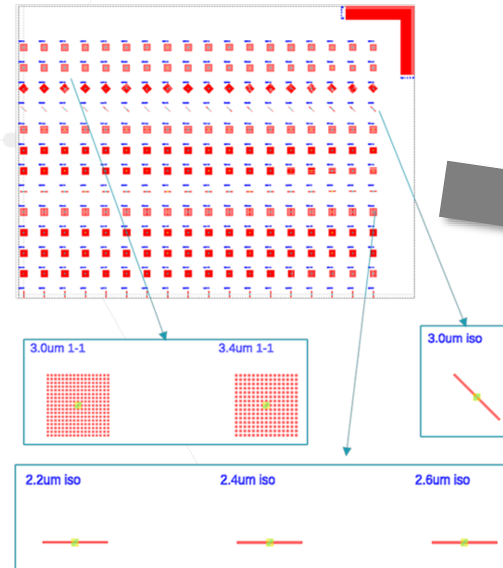


- Dedicated high performance MDP for mask house: hierarchy, parallel processing, mask process correction
- Strong for special Application like Flat Panel Display, Photonic IC, non-IC

Full Laser Process Calibration / Correction

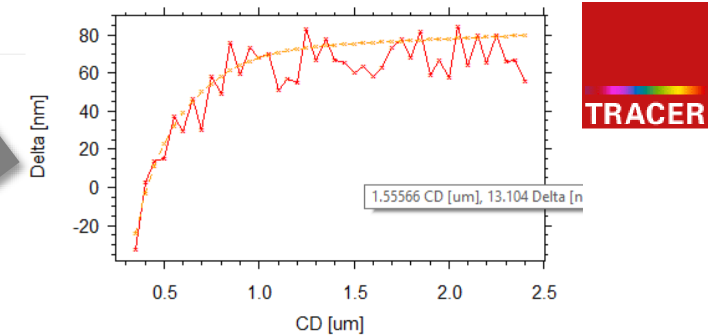
Typical Laser Mask Process Signature



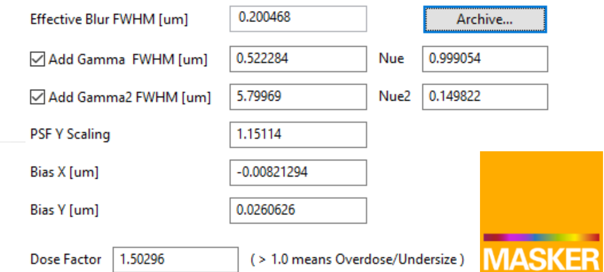


Expose and process the calibration pattern

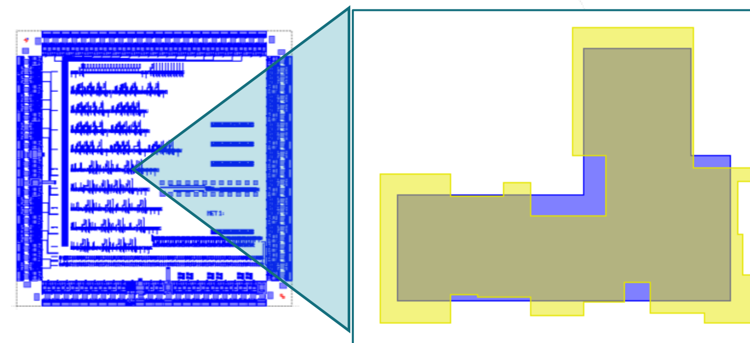
Measure results with CD-SEM (with the help of ProSEM)



Run calibration based on measured results

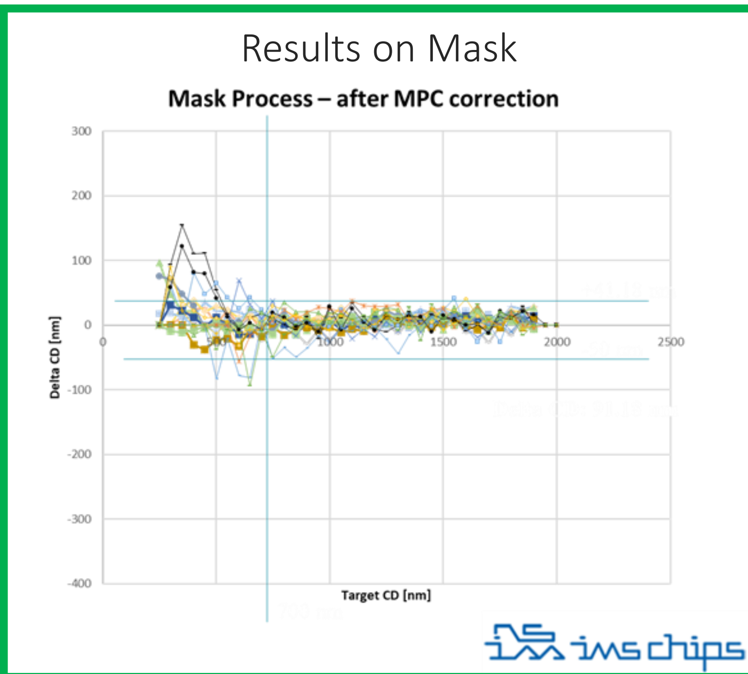


Run Model-MPC using input from TRACER

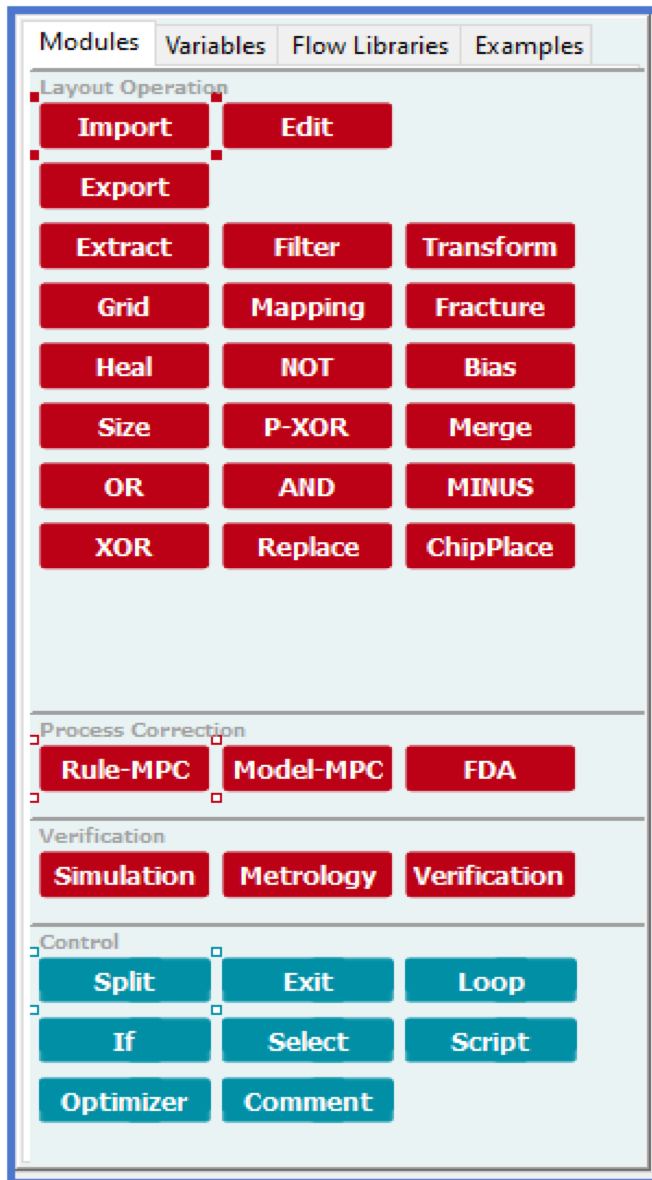


Correction results on target mask design

Results on Mask



What is MASKER



Powerful MDP & MPC for special applications with leading edge correction and verification capability:

- Includes all layout operations needed in a mask house production environment
- Optimized for low end IC and special masks (FPD, Photonics, IoT,…)
- Flexible Rule-MPC Features
  - Biasing (size, distance, density, angle, … dependent)
  - Serifs, hammerheads, scatter bar,… positioning
- Powerful Model-MPC
  - Laser exposure model
  - E-Beam exposure incl. advanced process effects
- Simulation of laser and e-beam exposure
- Verification including comparing layouts and DRC

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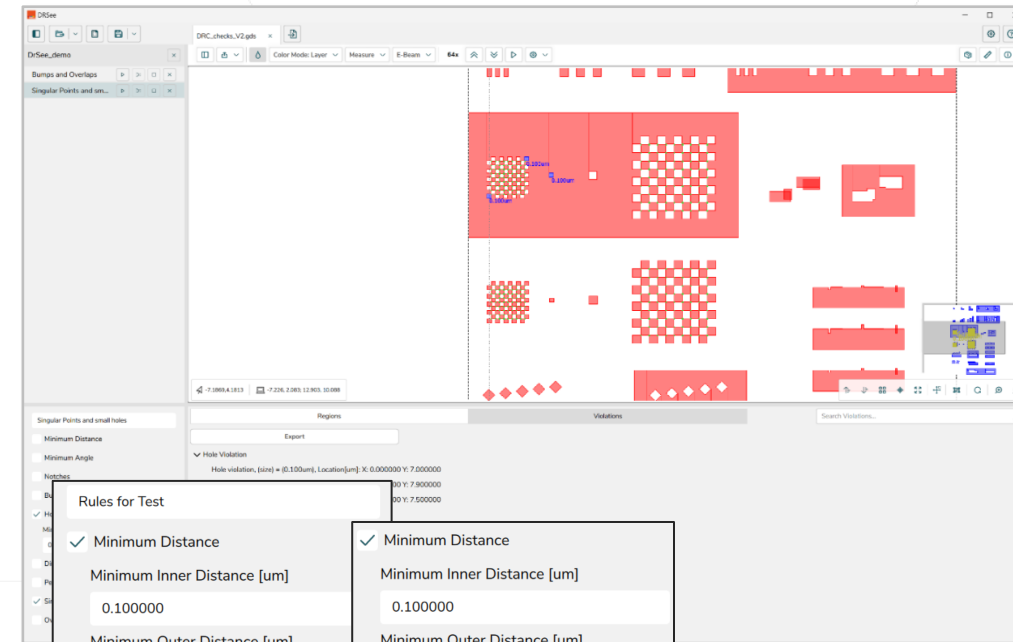
NEW DRSee – Design Rule Check

- Stand-alone software package
  - Fast, flexible and easy to use
  - Running on of-the-shelf HW with Linux or Windows
- Import of full chip/ mask layout data
  - Major layout formats (GDS, Oasis, Mebes, DXF,…)
  - Verification regions can be defined
- Comprehensive rule definition
  - Min. inner/ outer distance, angle
  - Notch, bump, hole, dimension
  - Perimeter, singular point, overlap
- Reporting of results
  - Display in layout viewer
  - List in violation table, search function
  - Data export in xml format

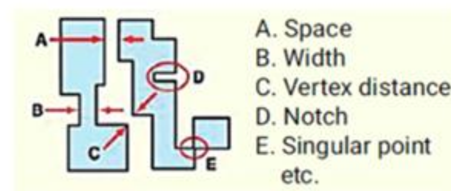


Rules for Test
Minimum Distance
Minimum Inner Distance [um]
0.100000
Minimum Outer Distance [um]
0.100000
Minimum Angle
Notches
Bumps
Holes
Dimensions
Perimeter
Singular Points
Overlap

Minimum Distance
Minimum Inner Distance [um]
0.100000
Minimum Outer Distance [um]
0.100000
Minimum Angle
Minimum Inner Angle [°]
85.000000
Minimum Outer Angle [°]
85.000000

Notches
Minimum Notch Size [um]
5.000000
Bumps
Minimum Bump Size [um]
5.000000
Holes
Minimum Hole Size [um]
0.400000

Dimensions
Minimum X-Size [um]
5.000000
Minimum Y-Size [um]
5.000000
Perimeter
Minimum Perimeter-Size [um]
9.000000
Singular Points
Overlap



GenISys – Your Solution Provider

GenISys offers “more than software”

- Application support including process (>10 application engineers)
- Experience from collaboration with >200 advanced nano centers
- Active community with >500 users exchanging at BEAMeetings world-wide
- Always at the „spearhead“ of technology with frequent updates
  - New features, enhancements, and fixes
  - All development is driven by users and equipment partners
  - Fast reaction on critical issues (patch within 24 hours)

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Thank You!

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